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IC Design: The Primary Competitive Advantage

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System Design

- There is a broad spectrum of design skills under the heading of System Design

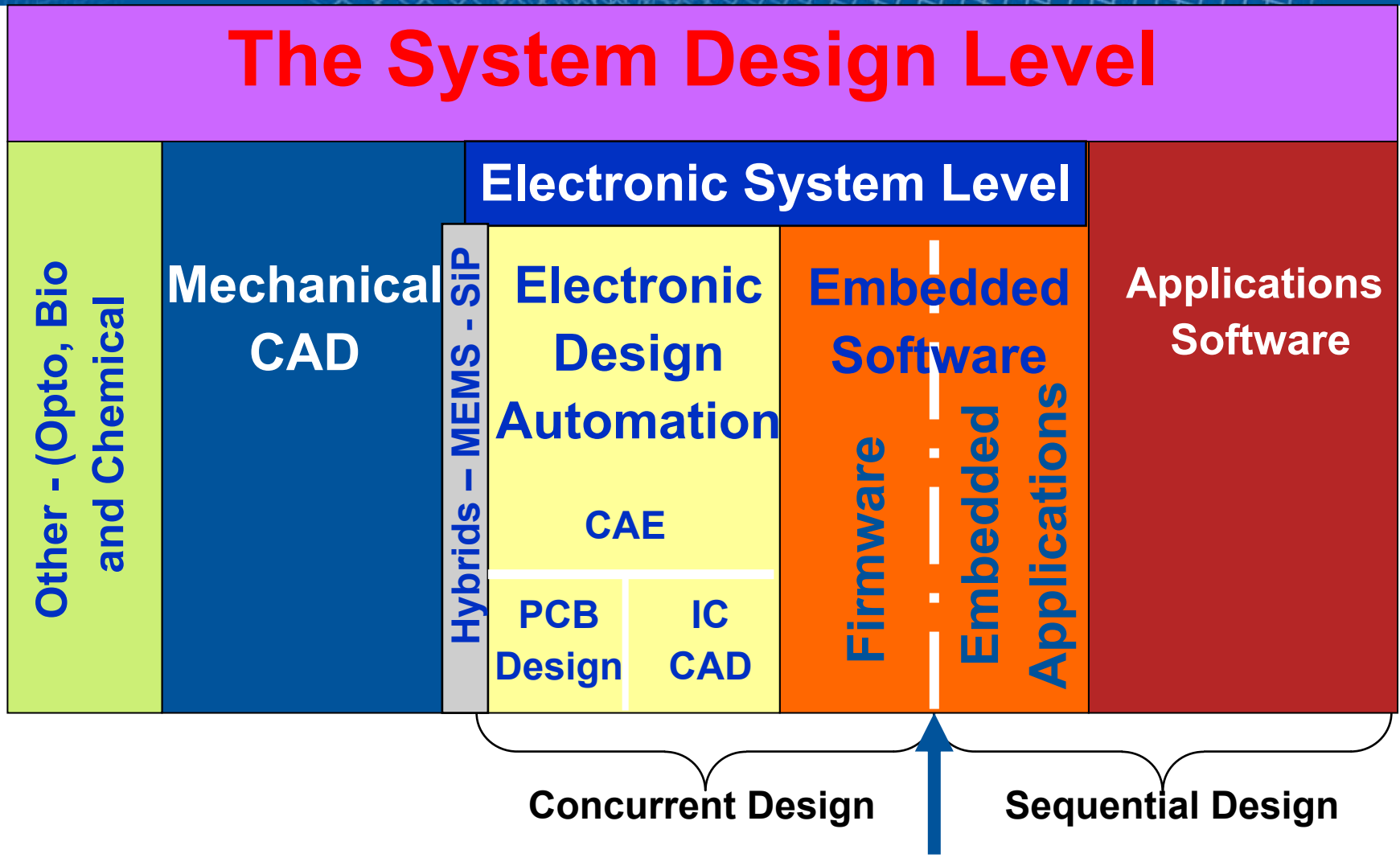
  - Applications Software development

  - Electronic System Design

  - Mechanical Design

  - and possibly Opto, Bio and Chemical Design

The Design Continuum



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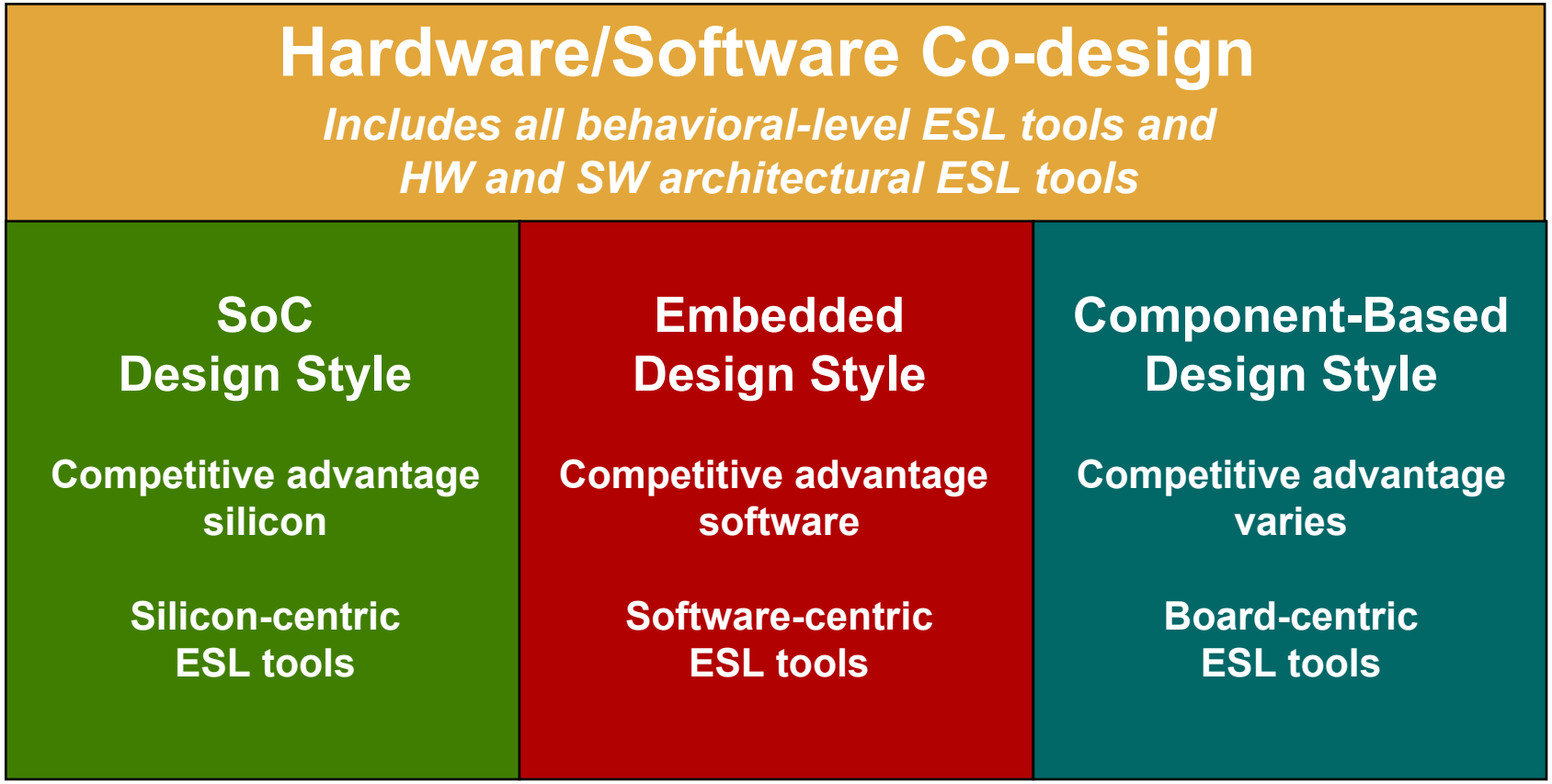
Styles of Electronic System Design

- There are three ways to Design an Electronic System.
  - Component Based Design
  - Embedded Design Style
  - SoC Design Style.

The ES-Level Landscape (Includes EDA and ESDT)



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Silicon Design Methodologies

- In Silicon Design we have progressed through three major design methodologies and are heading into a fourth.

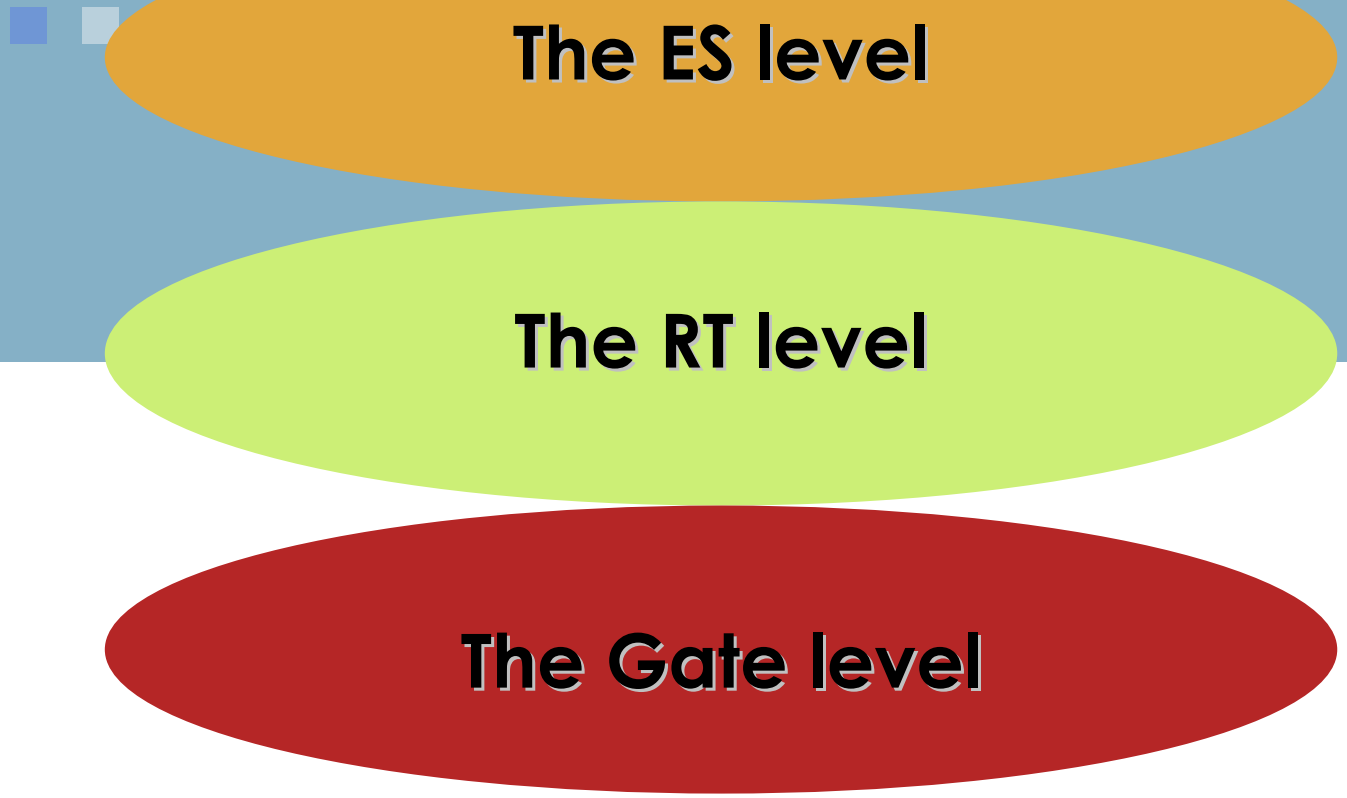
  - 1964 Transistor Level Design (IC CAD)

  - 1980 Gate Level Design (IC CAE)

  - 1987 Register Transfer Level Design (RTL)

  - 2005 Electronic System Level Design (ESL)

Semiconductor Design Methodologies



IC CAD

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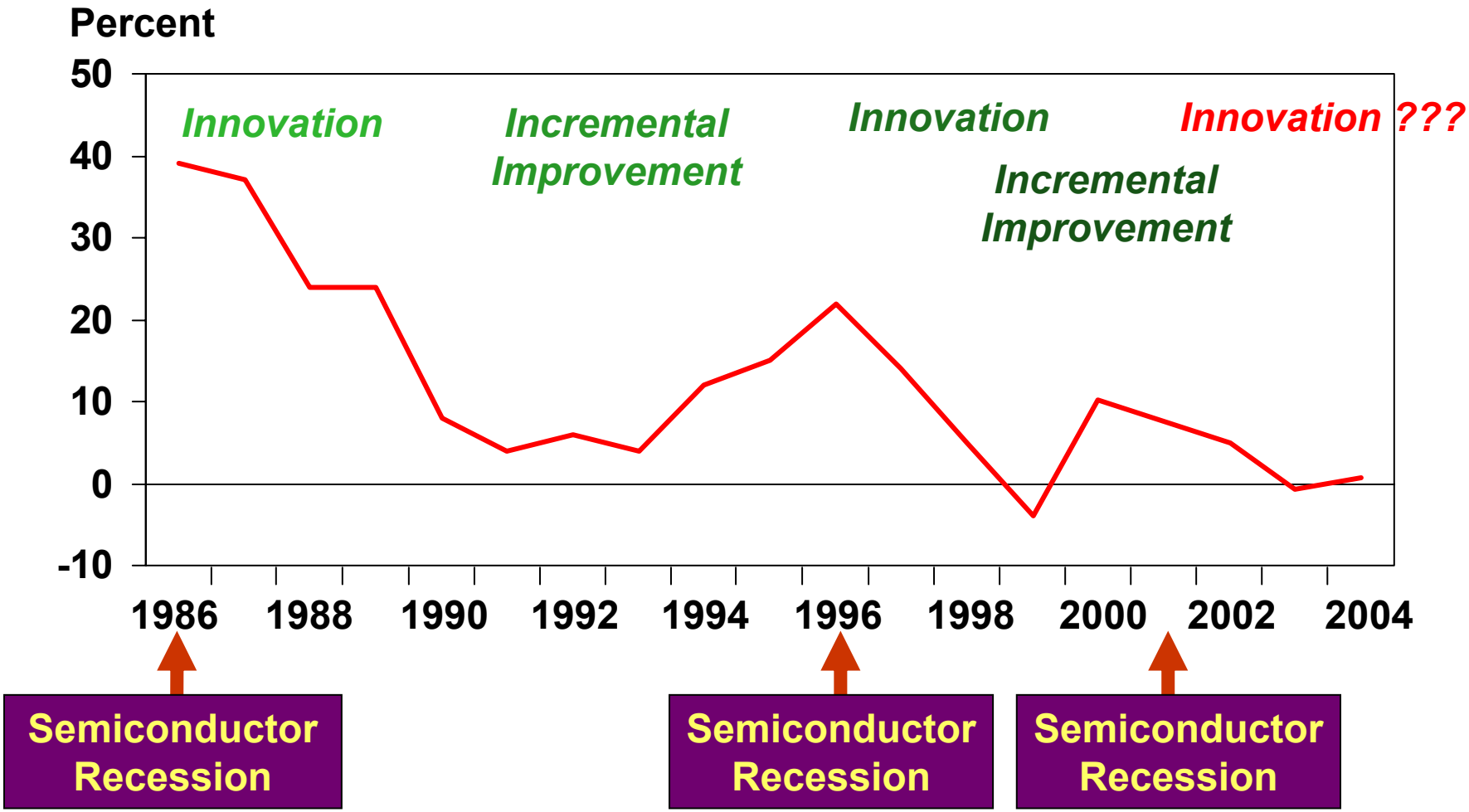
The Idea Cycle 2004 (as Measured by EDA Growth)



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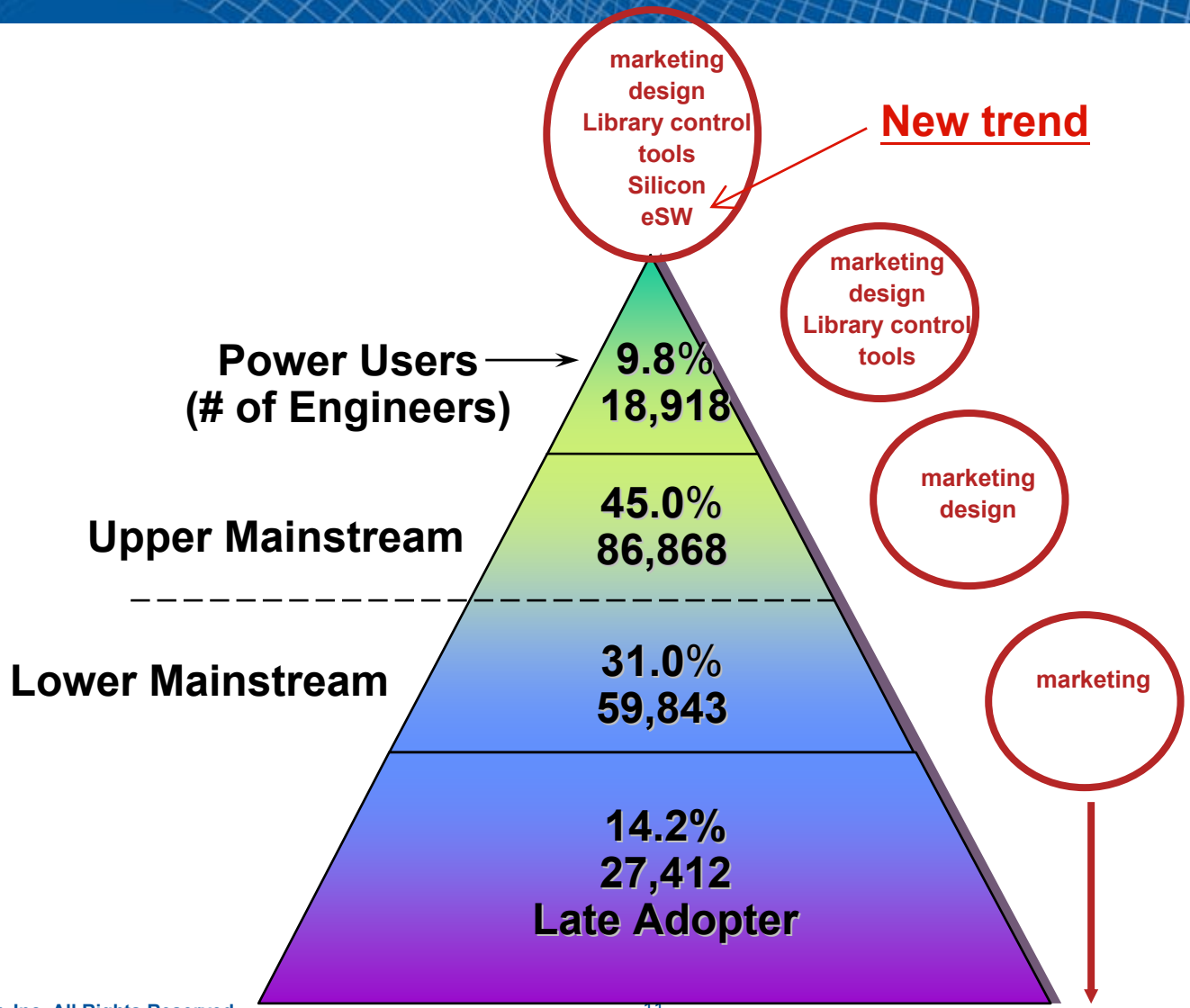
The Semiconductor Design Pyramid

- Indicates how design capability determines competitive advantage during the Incremental period of the Idea Cycle.
  - Power Users; top designers, large CAD groups, leading edge silicon, pushing the technology
  - Upper Mainstream User; good designers, CAD groups but little internal tool development, follows the Power User in silicon node and leading edge EDA tool use by two to three years
  - Lower Mainstream User; tends to use FPGAs, no CAD group, when using ASICs they tend to be two to three process nodes behind the state of the art.
  - Late Adopters – Little use of ASICs, tend to be all FPGAs or just off-the-shelf standard products.

The Semiconductor Design Pyramid 2005



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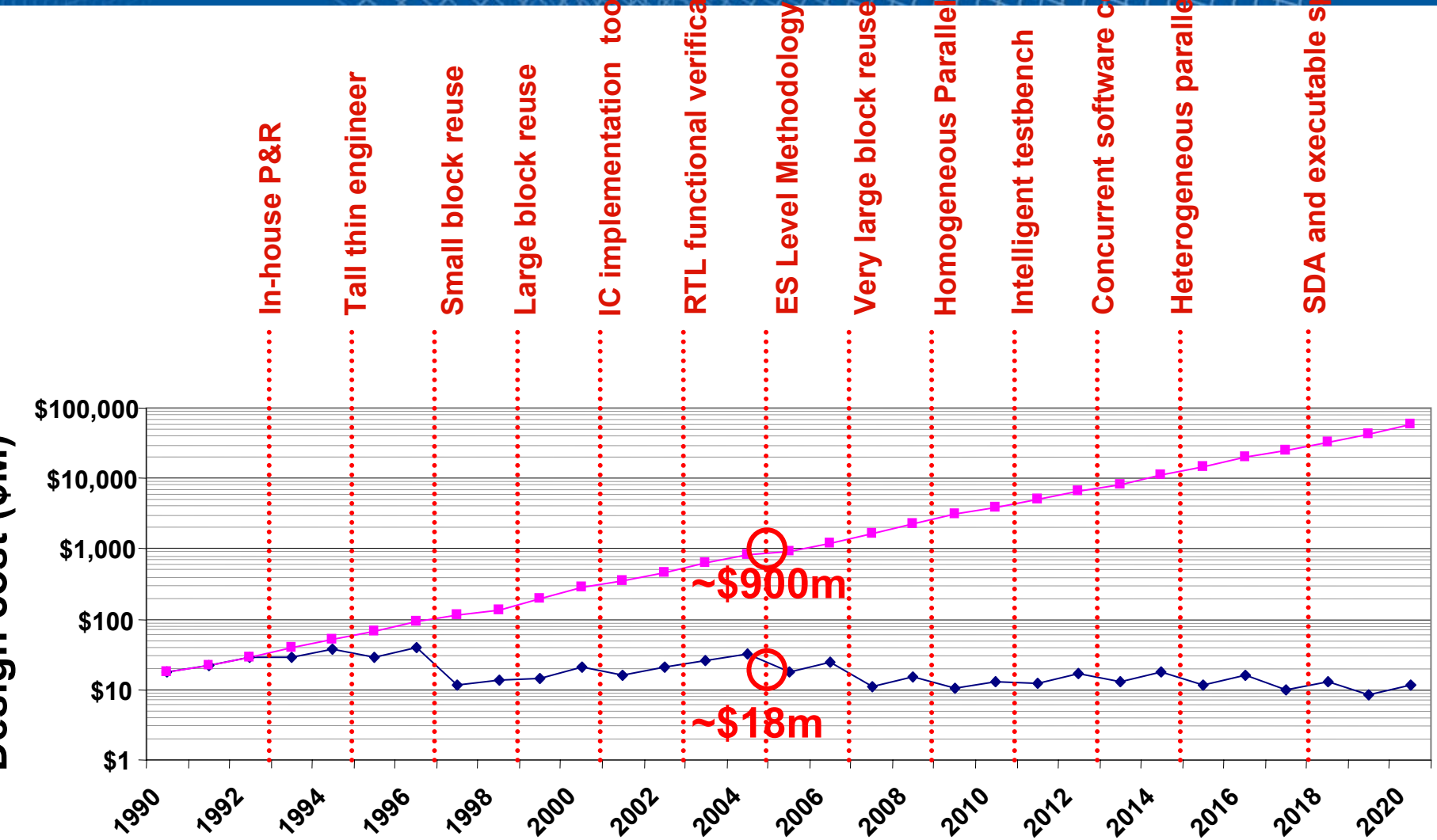
ITRS 2005



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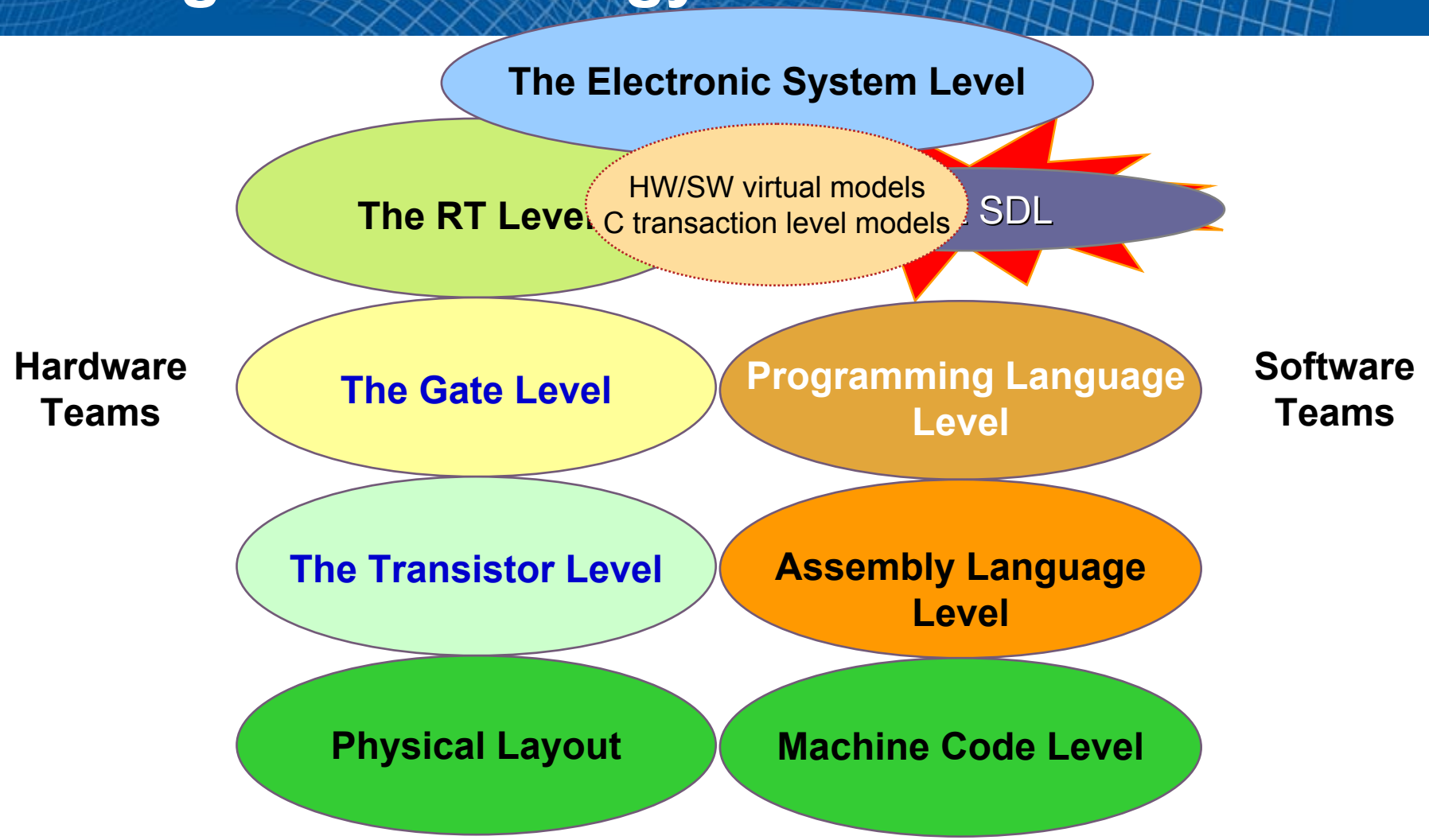
Productivity Improvements 1990 – 2001

DT Improvement	*Year*	*Productivity Delta*	*Productivity (Gates/Design-Year)*	*Cost of Component Affected*	*Description of Improvement*
None	1990		4K		
In-house place and route	1993	+38.9%	5.55K	PD Integration	Automated block placement and routing.
Tall Thin Engineer	1995	+63.6%	9.09K	Chip/circuit/PD Verification	Engineer than can pursue all required tasks to complete a design block, from RTL to GDSII.
Reuse—small blocks	1997	+340%	40K	Circuit/PD Verification	Blocks from 2,500–74,999 gates.
Reuse—large blocks	1999	+38.9%	56K	Chip/circuit/PD Integration Verification	Blocks from 75,000–1M gates.
IC implementation tool suite	2001	+63.6%	91K	Chip/circuit/PD Integration EDA support	Tightly integrated tool set that goes from RTL synthesis to GDS II through IC place and route.

Productivity Improvements 2003 - 2019

RTL functional verification tool suite	2003	+37.5%	125K	SW development Verification	RTL verification tool ("cockpit") that takes an ES-level description and partitions it into verifiable blocks, then executes verification tools on the blocks, while tracking and reporting code coverage.
Electronic system-level (ES-level) methodology	2005	+60%	200K	SW development Verification	Level above RTL, including both HW and SW design. It consists of a behavioral (where the system function has not been partitioned) and an architectural level (where HW and SW are identified and handed off to design teams).
Very large block reuse	2007	+200%	600K	Chip/circuit/PD Verification	Blocks >1M gates; intellectual-property cores
Homogeneous Parallel Processing	2009	+100-200%	1200K	Chip/circuit/PD Design and Verification	Many identical cores provide specialized processing around a main processor, which allows for performance, power efficiency, and high reuse
Intelligent Test Bench	2011	37.5%	2400K	Chip/circuit/PD Verification	Like RTL verification tool suite, but also with automation of the Verification Partitioning step.
Concurrent Software Compiler	2013	60%	3300K	Chip and system Design and Verification	Enables compilation and SW development in highly parallel processing SoCs
Heterogeneous Parallel Processing	2015	+100-200%	5278K	System Design and Verification	Each of the specialized cores around the main processor is not identical from the programming and implementation standpoint
System-level DA and executable specification	2017-19	+100-200%	10557K	System Design and Verification	Automates true system design on- and off-chip for the first time, including heterogeneous technologies.
TOTAL		+264,000%			

Design Methodology with eSW in 2005



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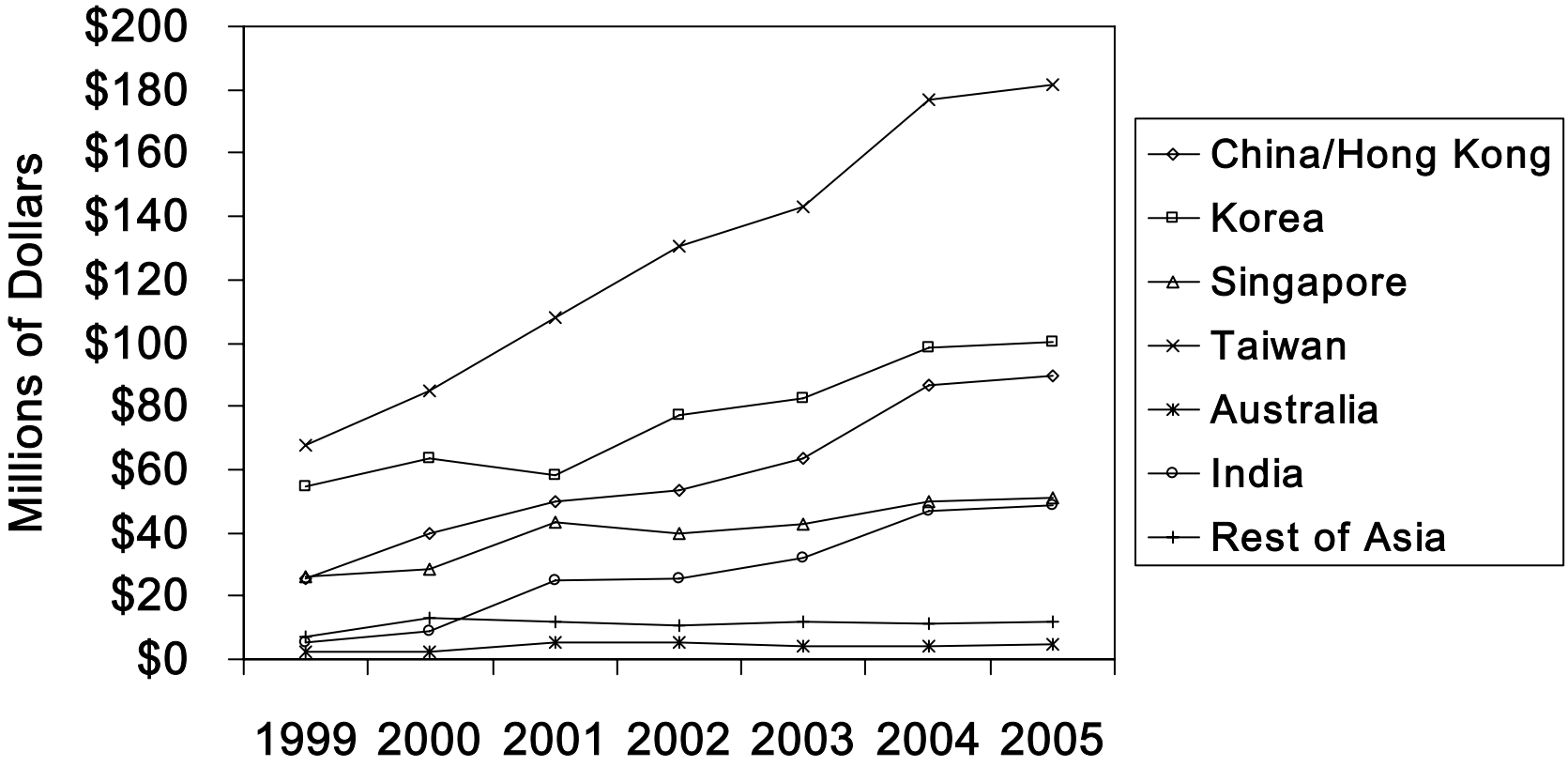
Asian EDA Spending by Country

Asia is the fastest growing region in EDA spending

EDA Spending by the Major Asian Countries

- Taiwan's Designers lead in Overall EDA Spending
- Taiwan leads in CAE with Korea a strong second - India has taken a big jump in CAE spending
- Taiwan has a commanding lead in IC CAD spending
- China is a strong number one in PCB spending

Total EDA Spending by Country



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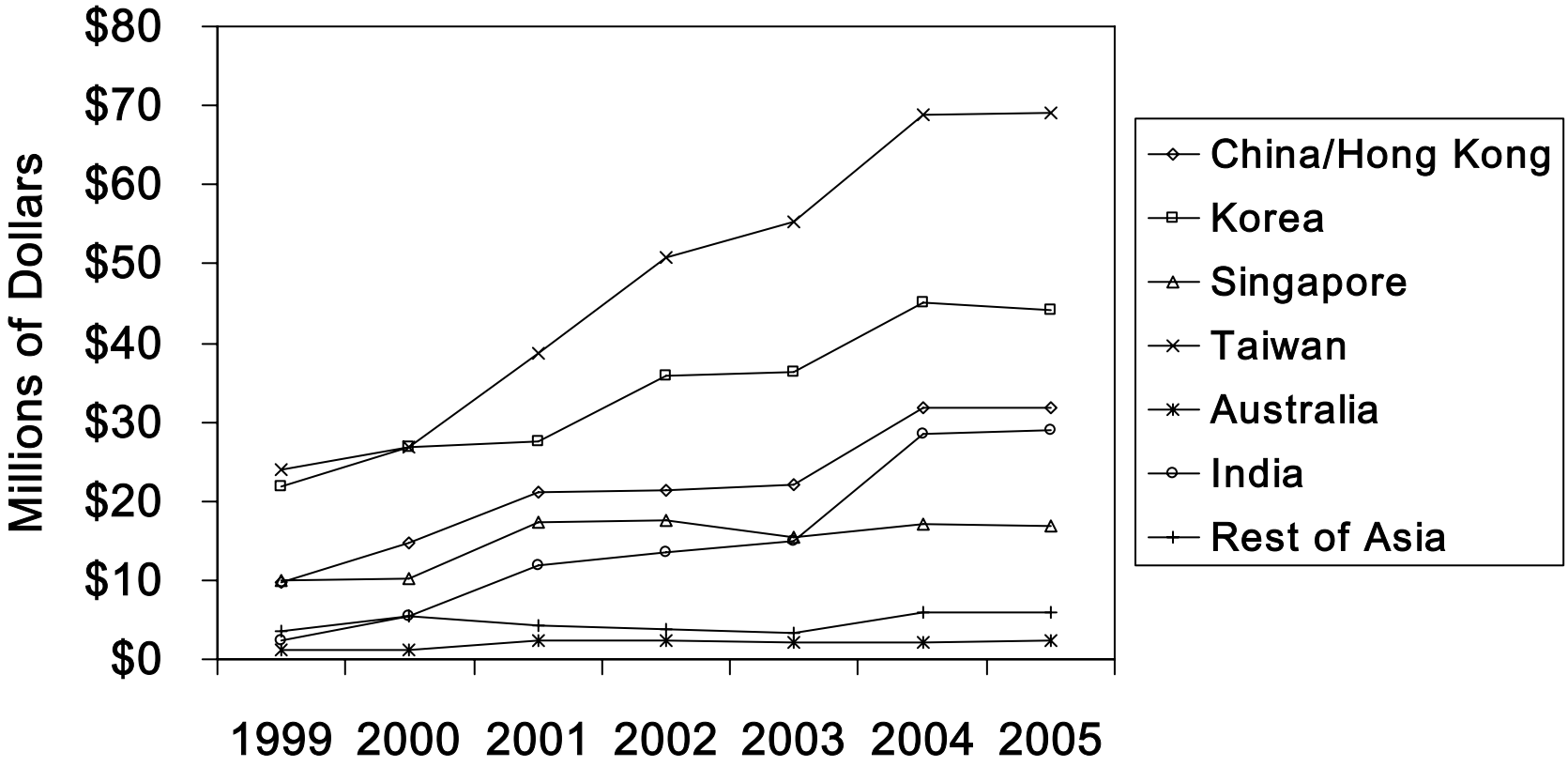
Total CAE Spending by Country



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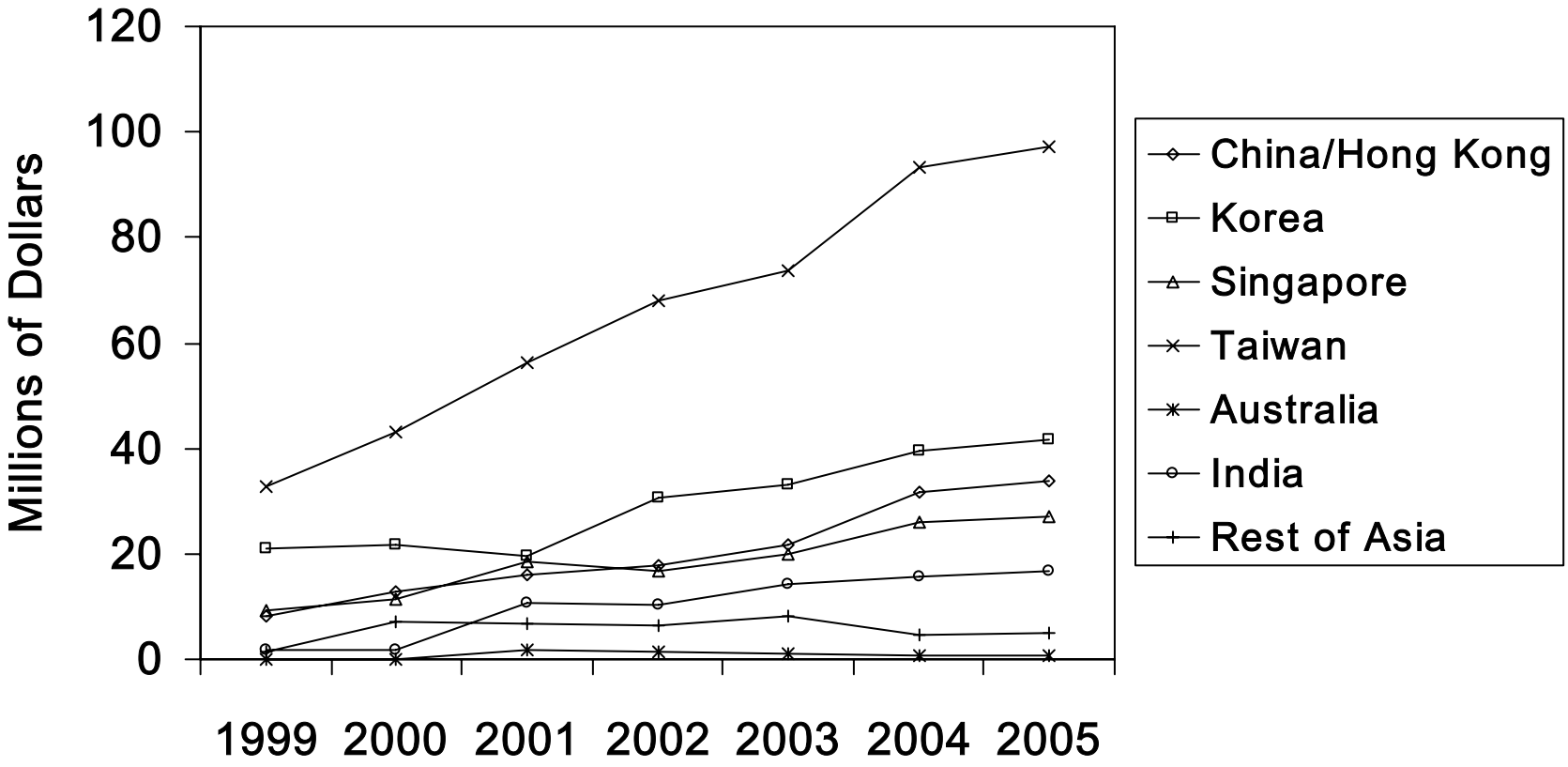
Total IC CAD Spending by Country



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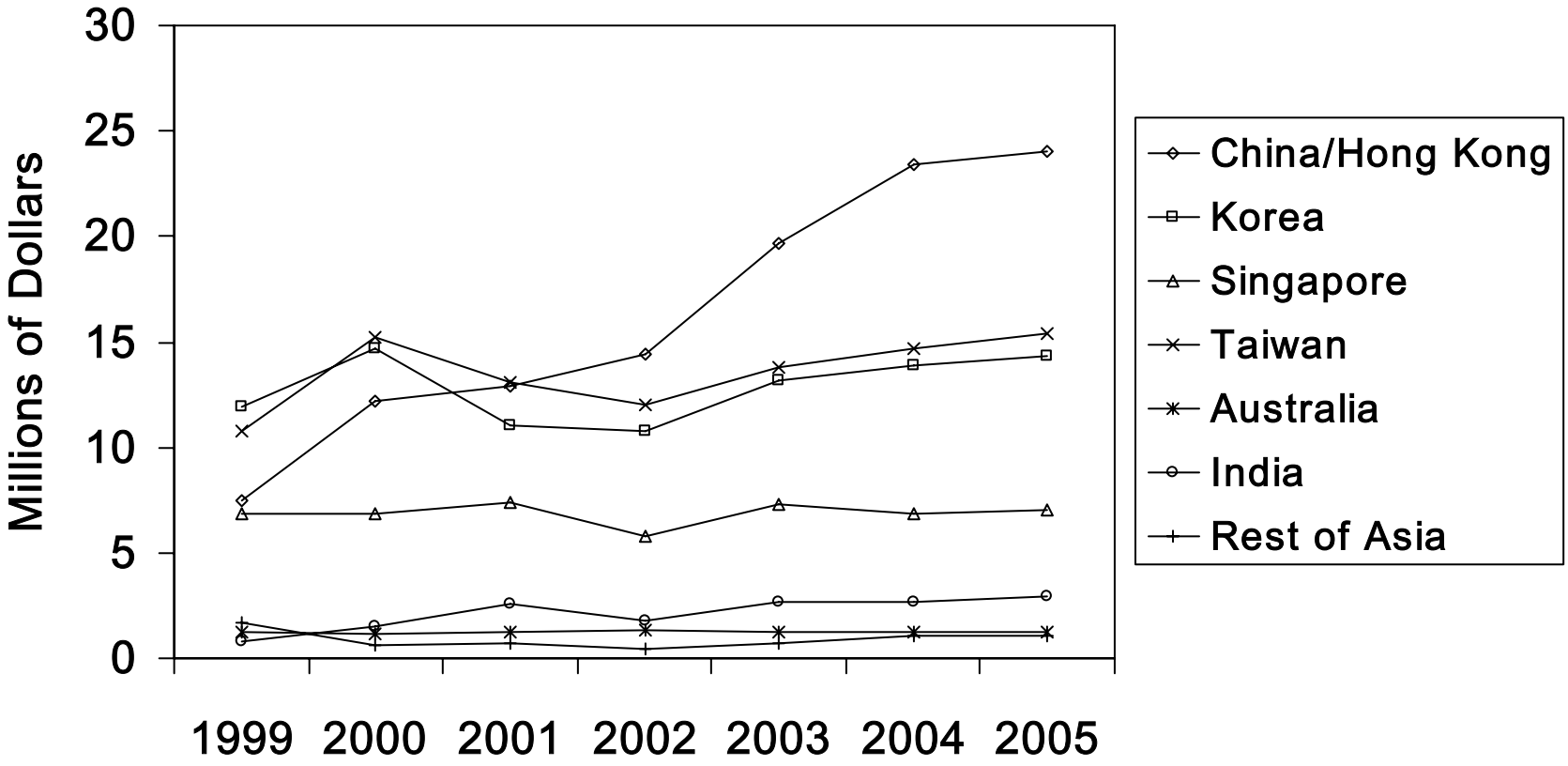
Total PCB Spending by Country



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In Conclusion

- Design is the number one competitive advantage.
- You must look at your market and determine if you need to be a Power User, a Mainstream User, or if a Late Adopter strategy will work.
- You must allocate your spending to build your Engineering and CAD teams as well as purchase your EDA tools to accommodate your strategy.

Any Questions ???

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